X-Band Monolithic Power Amplifier Using Low Characteristic Impedance Thin-Film Microstrip Transformers

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Abstract—**A technique is introduced for matching monolithic power amplifiers by using short thin-film microstrip transformers with very low characteristic impedance. An X-band power FET amplifier has been successfully realized with this technique, using a standard GaAs foundry two-level metal process. The amplifier has achieved over 5.5-dB small-signal gain and an output power of 1 watt at a center frequency of 11.3 GHz. This new matching technique can greatly reduce the area of the matching networks compared with conventional microstrip techniques which rely on cluster matching and power dividing/combining.**

I. Introduction

THE RECENTLY introduced thin-film microstrip (TFMS) technique has successfully been applied to the miniaturization of branch-line couplers and a range of novel circuits [1], [2]. In this technique, multiple metal layers and thin dielectric films are deposited onto the wafer, and the thin dielectric films serve as the "substrate" for miniature microstrip lines. The increased packing density this allows is considerable, and 50-Ω lines have a typical width of only 10 μm. In this letter, the thin-film microstrip technique has been extended to realize transmission lines with characteristic impedance as low as 3.5 Ω. For such low impedances, conventional microstrip on thick substrates would be too wide and would suffer frequency limitations due to transverse modes. Hence, in power amplifier matching networks, conventional microstrip transformers are unrealizable when the device input and output impedances are very low, and so power dividing/combining and cluster matching techniques are usually employed [3], [4]. TFMS lines thus have an important application as they overcome this characteristic impedance limit. The amplifier presented here uses the standard GEC-Marconi (Caswell) foundry F20 process, which offers 0.5-μm gate-length ion-implanted MESFET's and through-GaAs via holes. This process employs two metal layers separated by a thin polyimide film, so that spiral inductors have underpasses rather than air-bridges. Using this feature, low impedance TFMS lines can be realized on this well-qualified standard process, without additional fabrication steps. The characterization of these low characteristic impedance lines is now described, followed by the design and performance of the prototype X-band power FET amplifier using the new matching technique.

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II. TFMS Characterization

Standard microstrip design packages are found to give very large errors in calculating TFMS electrical parameters because the small dimensions are outside their range of validity. In order to obtain the TFMS parameters, four different widths of line were fabricated with strip widths of 10, 20, 60, and 120 μm. These were then measured up to 40 GHz using a Cascade Microtech™ prober and HP8510B™ network analyser. A model for the transmission line and the CPW-TFMS transition was then fitted to each set of measured data, using the Touchstone™ package. The resulting graph for characteristic impedance versus strip width is shown in Fig. 1. The main potential drawback with TFMS lines is the increased loss, but in fact the 120-μm line has a measured loss of only 0.36 dB per millimeter at 11 GHz. For narrow lines the increased loss is more serious, and the 10-μm line has 2.1-dB loss per millimeter at 11 GHz. For higher Z_o with low loss, it is necessary to increase the dielectric thickness rather than make the tracks narrower. ATR [5] have used three layers of a 3-μm dielectric in order to achieve acceptable loss in 50-Ω TFMS lines, and have also reported valley microstrip lines for reduced loss [6].

III. Circuit Description

As the design was on a multiproject wafer it was not possible to use the medium-power foundry process offered by Caswell, nor the high-power R & D process with bath-tub vias. Hence, the design involved several trade-offs, and whilst the results presented here serve to demonstrate the new matching technique, care must be taken in comparing the actual power, gain, and efficiency with those achieved elsewhere. Four individual 8 × 175-μm devices were used, connected with a short microstrip feed network. This topology was chosen for several reasons; firstly in order to be able to use standard foundry device models, secondly to ensure equal path lengths to each device, and thirdly to ease the thermal problems encountered with a single large device. The microstrip feed lines were made as short as possible, and are not intended to contribute significantly to the matching process. This FET and microstrip feed structure was modeled using small-signal

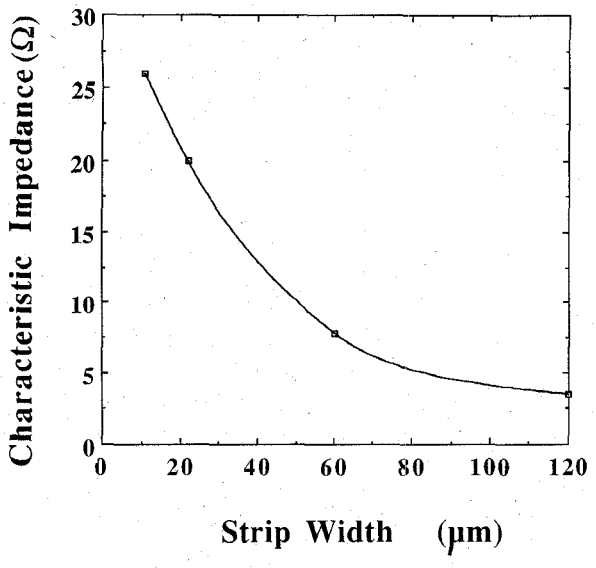

Fig. 1. TFMS characteristic impedance for different strip widths.

foundry data in order to find the input and output impedances for maximum available gain at 11 GHz. The short impedance transformer technique was then used to match these to 50 Ω. In this standard technique, a device impedance $R + jX$ can be matched directly to Z_o by selecting the transformer characteristic impedance Z_T and electrical length θ such that

$$Z_T = \sqrt{Z_o R - \frac{X^2 Z_o}{Z_o - R}}, \quad \text{for } X^2 < R(Z_o - R) \text{ and } R \neq Z_o \quad (1)$$

and

$$\theta = \arctan\left(\frac{Z_T(Z_o - R)}{X Z_o}\right). \quad (2)$$

This matching technique is more compact than the quarter-wave transformer, but often requires unrealistic values of Z_T. For this amplifier the required input and output transformer impedances were found to be 4 Ω and 8.8 Ω, respectively, and the input and output electrical lengths 22.4 and 40.6 degrees, respectively. These values gave the required initial values of transformer width and length. The complete amplifier with dc bias circuitry was then simulated and the small-signal performance optimized. A microphotograph of the 3.0 × 2.0-mm amplifier chip is shown in Fig. 2. The TFMS transformers and their ground planes can be clearly seen.

IV. Measured Performance

Initial attempts to measure the circuit were thwarted by a low-frequency oscillation problem. This was found to be because the on-chip decoupling of the drain bias stub was insufficient, and supplementary off-chip decoupling could not solve the problem because of the inevitable bond-wire inductance. Hence, the following results were obtained by applying the drain bias through a bias-tee. The small-signal response, measured with the prober and HP8510B (with attenuation), is shown in Fig. 3. The gain is over 5.5 dB at the center frequency of 11.3 GHz. The output match is excellent at better than 25

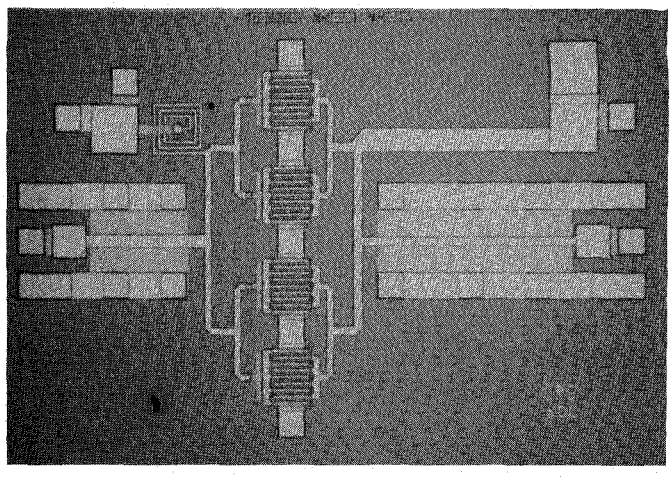

Fig. 2. Microphotograph of the power amplifier chip.

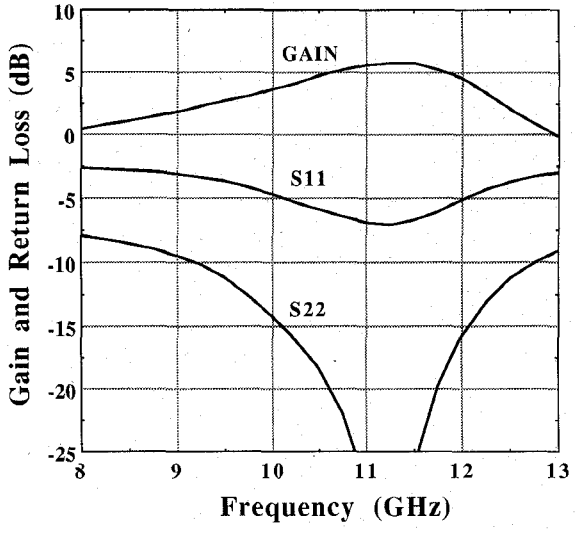

Fig. 3. Measured small-signal gain and return loss responses.

dB, and the input match is 7 dB at the center frequency. The maximum available small-signal gain of the FET with its feed network was predicted to be 7.8 dB. The 2.3 dB gain reduction can be attributed to mismatch loss at the input (1 dB), and by loss in the input and output TFMS transformers (0.4 dB and 0.9 dB, respectively). Spot frequency power measurements were made using a power meter and a TWT driver amplifier fed from an HP8350 sweep generator. The power transfer characteristic measured at 11.3 GHz is plotted in Fig. 4. The output power is just over 1 watt at 1-dB gain compression, and the power-added efficiency is 18.9 %. These results are as expected for the low-noise FET process. The GEC-Marconi foundry power device could achieve almost double the power for the same gate periphery, and much higher efficiency.

V. Conclusion

The realization of ultra-low impedance transmission lines using the thin-film microstrip technique has been described, and their application to power FET matching networks has been demonstrated for the first time. This first prototype amplifier has achieved a small-signal gain of 5.5 dB at 11.3

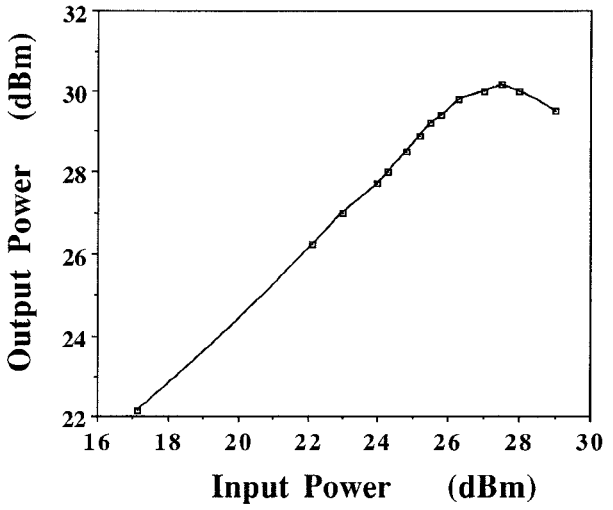

Fig. 4. Input–output power transfer characteristic measured at 11.3 GHz.

GHz and 1-W output power. There is considerable scope for improving the performance by using the foundry power FET process, by the possible inclusion of bath-tub vias, and by optimization of the FET layout. For example, the "serpentine" FET structure [7] could be used for improved heat dissipation, and the feed network minimized. By optimizing the FET topology and using the TFMS short transformers introduced here, very compact monolithic power amplifiers can be realized by removing the need for large microstrip power dividing, combining, and matching networks.

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